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~~(EECS2021E) Chapter 5 Cache Part~~

† What is CACHE MEMORY? What does

CACHE MEMORY mean? CACHE

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Coherence Problem | Solution to

Cache Coherence | Why Updation?

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Architecture SOLUTION INTR is a

signal which if enabled then microprocessor has interrupt enabled it receives high INR signal & activates INTA signal, so another request can ' t be accepted till CPU is busy in servicing interrupt. Hence (A) is correct option. Question. 12

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